Store Into Instruction Stream: Searching for the Culprits to Save CPU

Scott Chapman

scott.chapman@epstrategies.com

Enterprise Performance Strategies

November 2021

Session 6BH

GSE UK Conference 2021 Charity Raffle

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Abstract

- CPU overhead caused by the programming anti-pattern of updating data that's too close to the instruction stream has long been a known problem. IBM came out with a nice formula that highlights time intervals where that may practice may be causing significant overhead. But that's only part of the battle: the next question is how do you find the possible culprits so you can remediate them?

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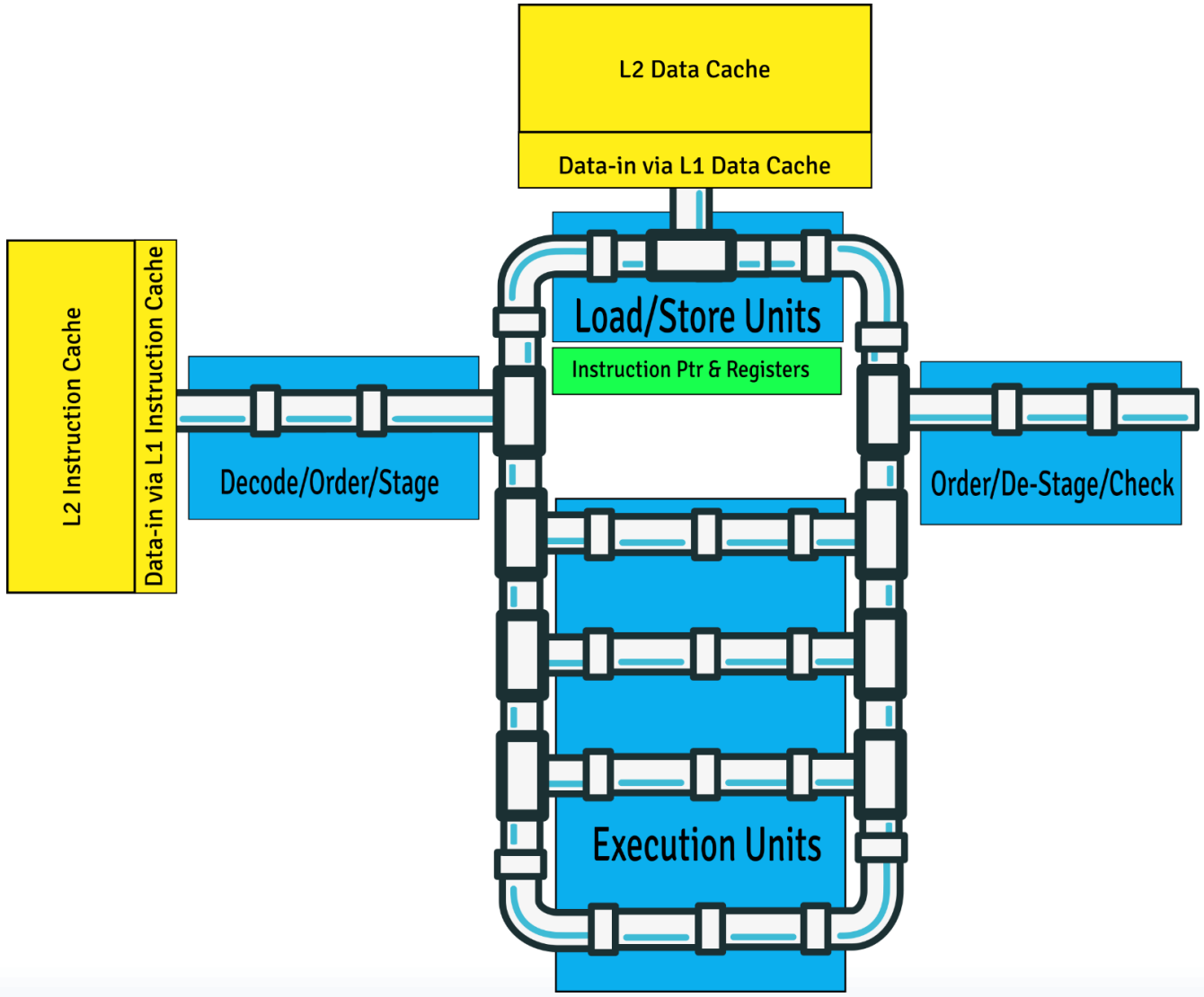
Store Into Instruction Stream

Modern Superscalar Processors

- Modern processors are complicated
- The appearance that program instructions happen in order as written is a fiction maintained by the processor
  - Many instructions will execute out of order
- Multiple instructions in-flight at any moment
- Aim: 1+ instruction finished / cycle
- Lots of things can cause pipeline stalls
  - L1 / TLB misses
  - Branch prediction misses
  - Data dependencies
  - Long instructions
- When stalled, there are parts of the chip idle (not doing work)
  - Out-of-order execution helps avoid pipeline stalls



SIIS

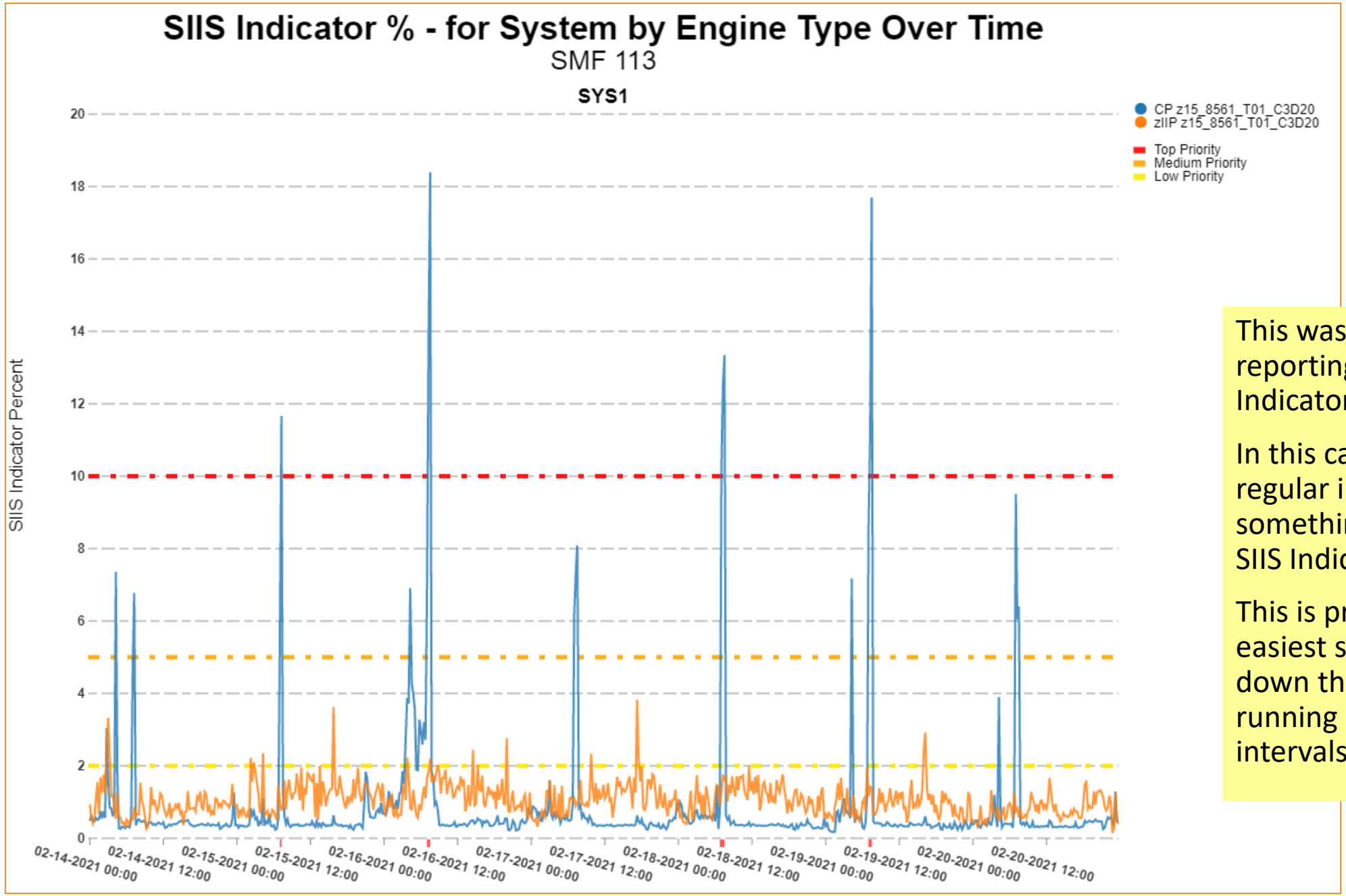
- Store Into Instruction Stream (SIIS) describes a situation where code writes to memory that is within 1 cache line (256 bytes) of the executing instructions
  - That update will trigger a flush of that cache line from the L1 Instruction cache, which will trigger a pipeline flush
  - This can be a significant performance hit!
  - Obviously doing this once is not a noticeable problem, but doing it repeatedly can be
- Primarily is seen in programs written in Assembler
  - FORTRAN protected against this since about 2002
  - COBOL v4.2 issue only when compiled with NOOPT and/or TEST options, which should not be the case for production code
    - If you have production code with NOOPT/TEST, SIIS is probably the least of your inefficiencies

Do you have a SIIS problem?

- See: https://www.ibm.com/support/pages/node/6355777
- The IBM formula is effectively the percentage of instruction stream updates that required L3 intervention
- IBM thresholds for recommended action:

SIIS Description	SIIS Indicator %	Action
Noise – it will never be 0%	< 2%	None
Minimal SIIS impact	2% < 5%	Low Priority but potential MSU savings
Noteworthy SIIS impact	5% < 10%	Medium Priority – Investigate and Remediate
Considerable SIIS impact	>= 10%	Top Priority – Investigate and Remediate

- Note that this doesn't estimate the actual savings
  - In some cases that can be significant
  - In some cases you can have high SIIS % during low-utilization times
- How do you find the culprit(s)???



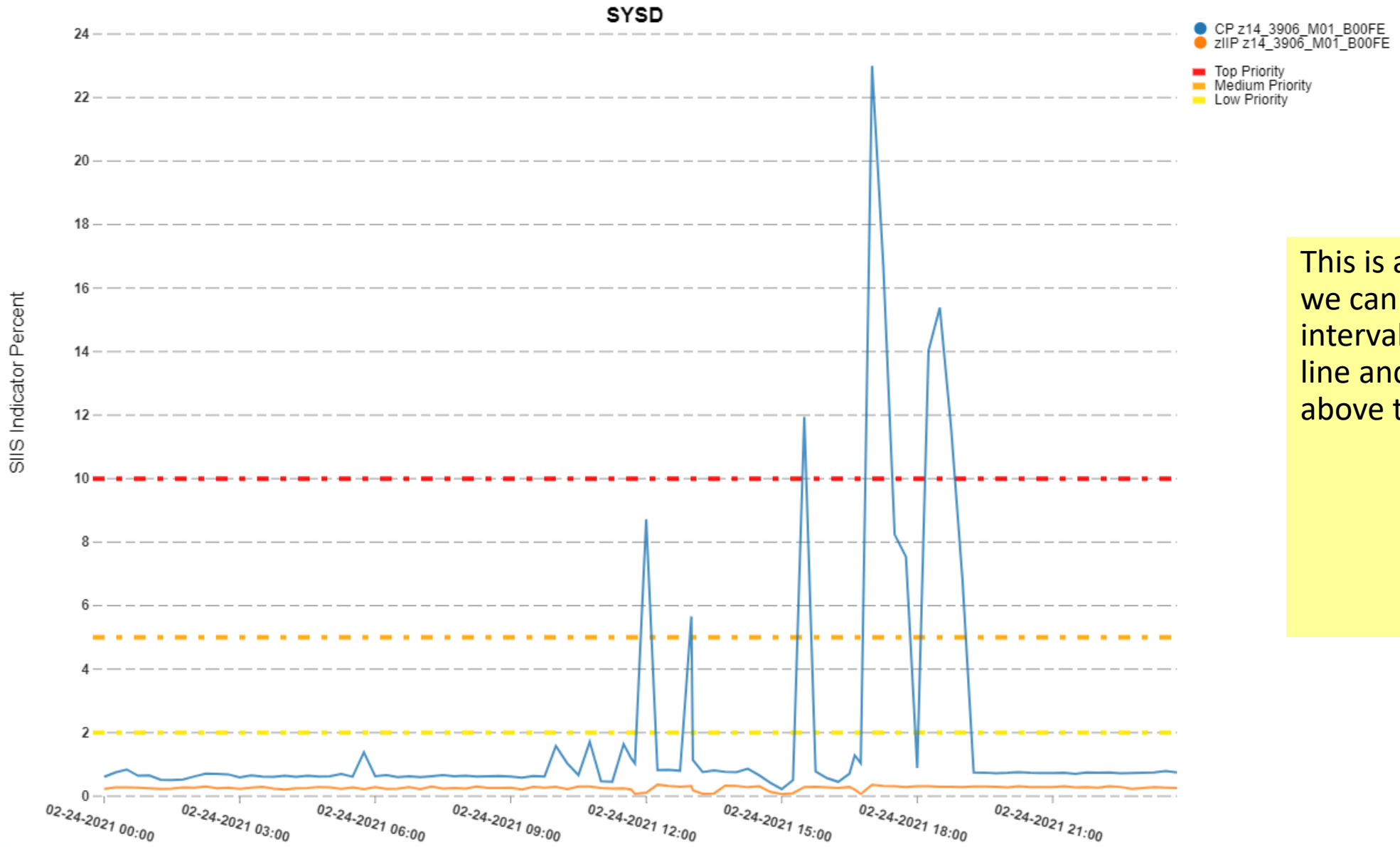
This was our initial reporting of SIIS Indicator %.

In this case there's a regular instance of something triggering the SIIS Indicator high.

This is probably the easiest scenario to track down the culprit: what's running during those intervals?

SIIS Indicator % - for System by Engine Type Over Time

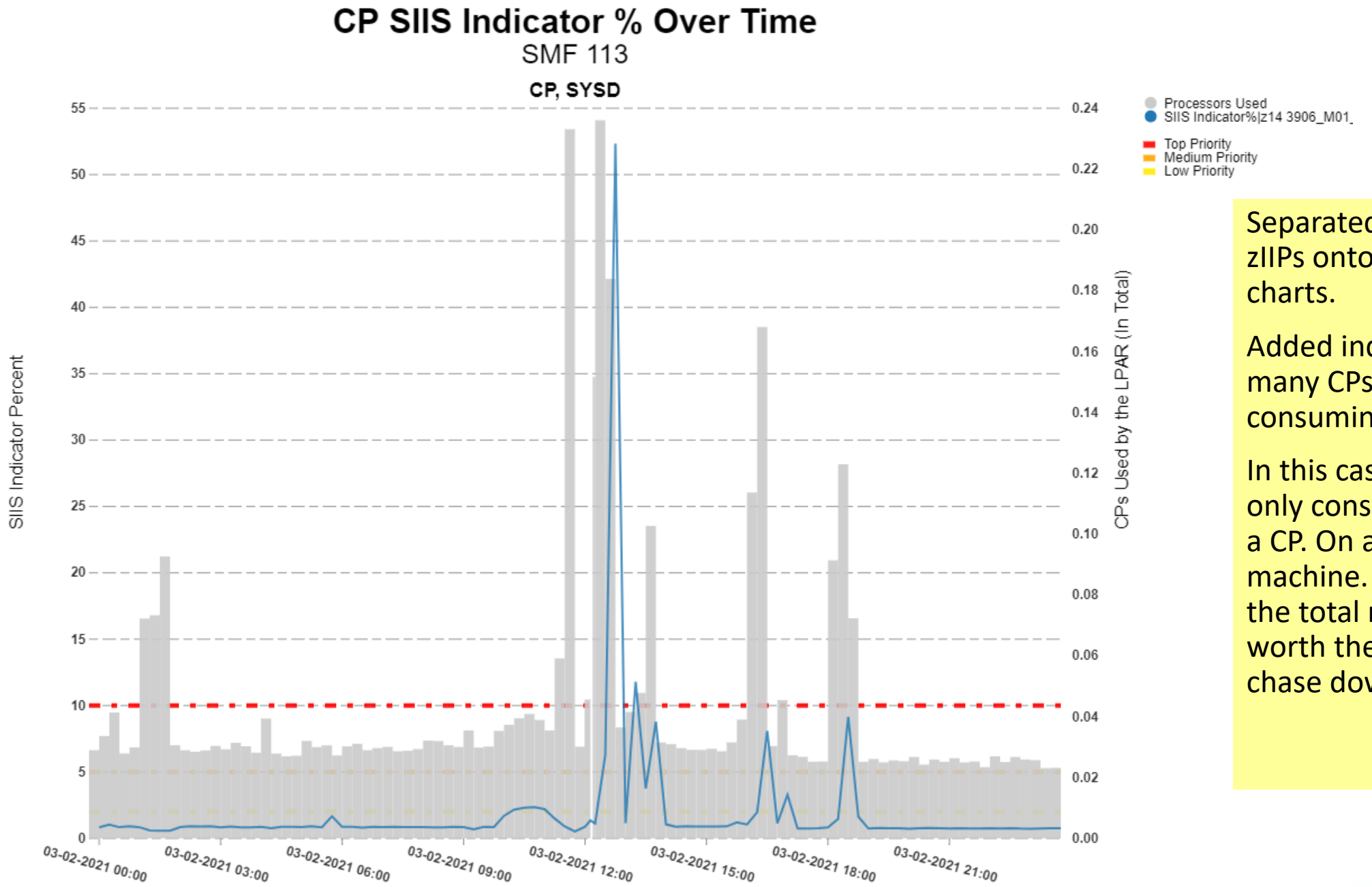
SMF 113



This is a single day but we can see multiple intervals above the 10% line and some more above the 5% line

SIIS Reporting Issues

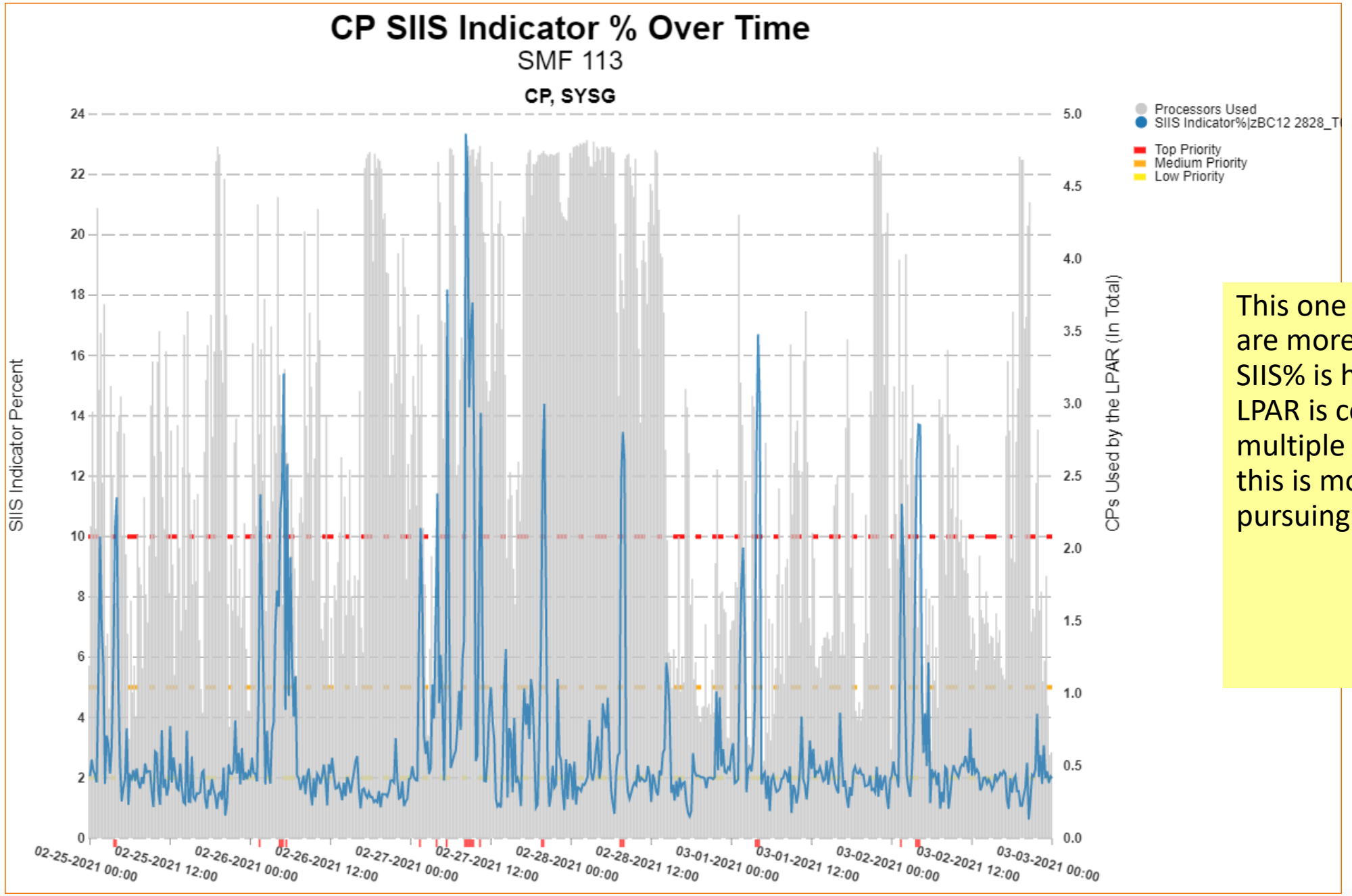
- How much savings are we really talking about?
  - Is it going to be worth the time and trouble of tracking down the culprits?
- Do we really care about SIIS on zIIP engines?
  - Probably not since zIIPs are cheaper and generally more abundant
  - And any Assembler code running on zIIPs is going to be coming from ISVs
- How can we find the culprits?
  - Look for commonly running assembler-based programs in problem times
  - Look for high CPIs in problem times? (Using the SMF 30 instruction counts)
- So we made some reporting changes…



Separated out CPs and zIIPs onto their own charts.

Added indicator for how many CPs the LPAR is consuming (as a whole).

In this case the LPAR is only consuming <20% of a CP. On a 6-way machine. So about 3% of the total machine. Is it worth the trouble to chase down?

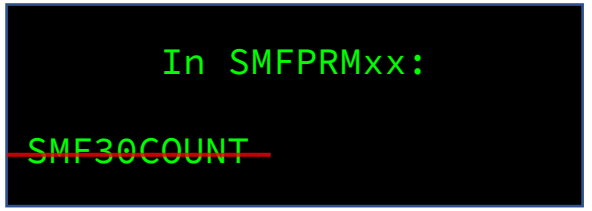


This one looks like there are more intervals where SIIS% is high and the LPAR is consuming multiple CPs so maybe this is more worth pursuing.

SMF 30 Instruction Counter

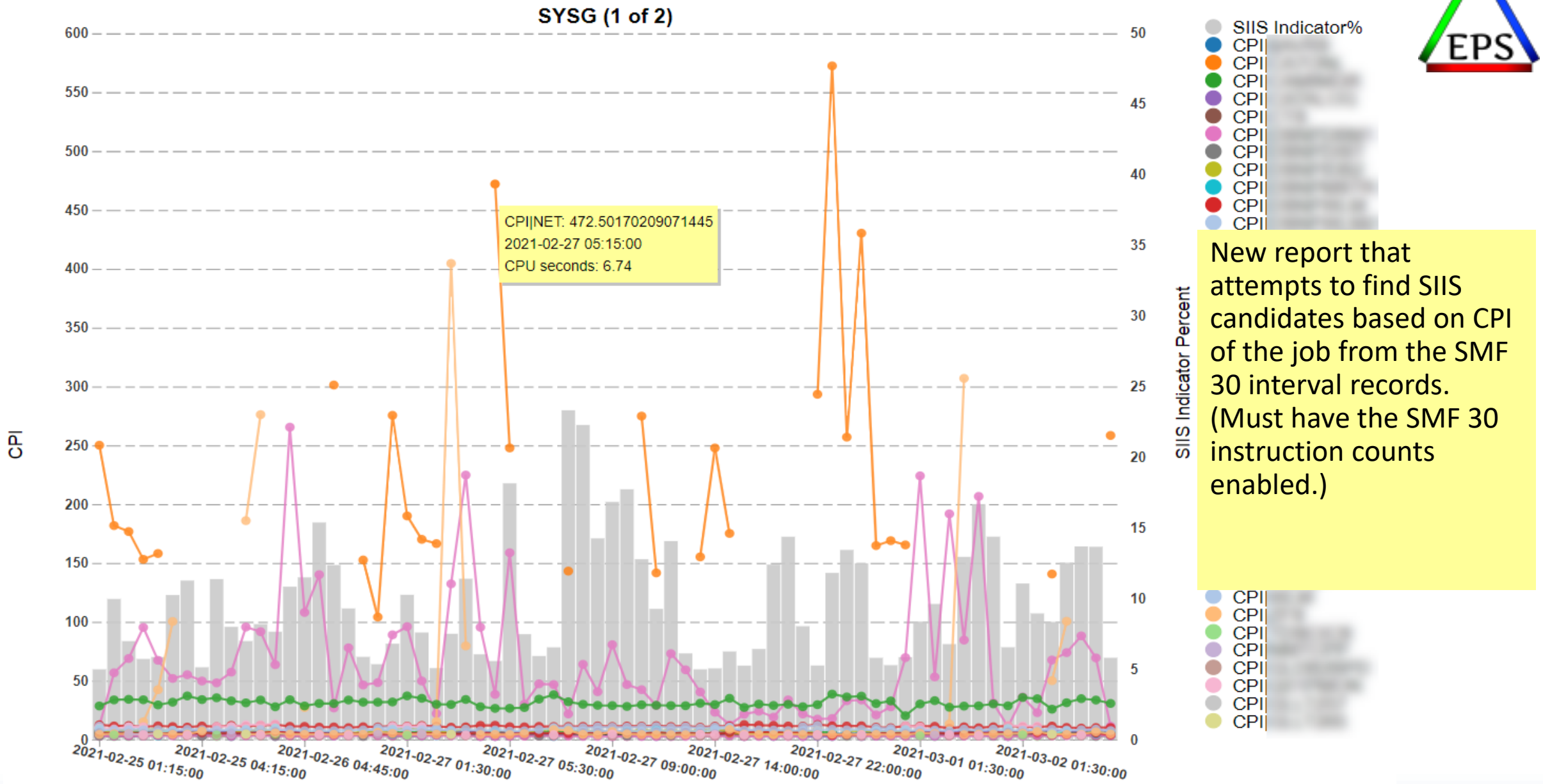
- SMFPRMxx option SMF30COUNT enables the SMF 30 Counter Data Section
  - Default is NOSMF30COUNT
- The idea for these counters was that while CPU time is variable due to things like cache contention, the number of instructions being executed should be stable, so maybe that would be a better measurement to use
- Except it ended up not being stable
  - CPU timers subtract out interrupt handling time
  - There's no similar mechanism for backing out interrupt handling instructions
  - So the instruction counts are potentially more variable than CPU time
- So even though section is relatively small, why bother?
  - Recommendation: don't use this

Time to revisit this?!?



SIIS - Job Name Candidates

(Job Name from Step EXEC=)



New report that attempts to find SIIS candidates based on CPI of the job from the SMF 30 interval records. (Must have the SMF 30 instruction counts enabled.)

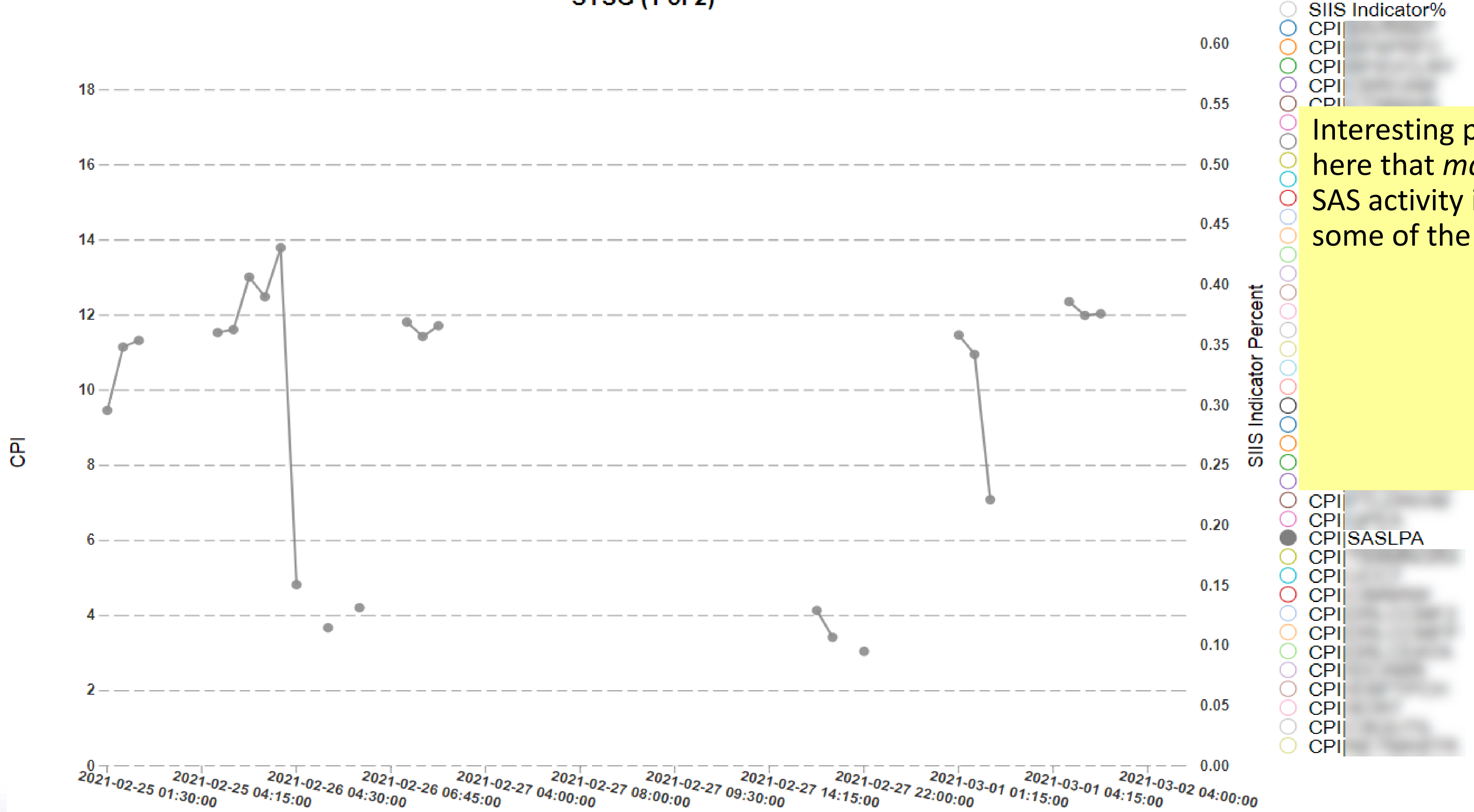
SIIS Culprits report

- Note that there were several address spaces that had really high CPIs!
  - NET, *DBM1, OAM
  - Commonality: compression and encryption
  - Compression and encryption instructions will naturally take many cycles to complete so address spaces making heavy use of these will have high CPIs
  - This is not indicative of a problem!
- Note that if you hover over a point you get the CPU time consumed by that address space in that interval to help you determine if you want to pursue
  - High CPI with low CPU usage = immaterial (low usage could cause high CPI)
- Look for things that appear in multiple intervals
  - And are written in Assembler
- Also have the report by PGM=

SIIS - Program Name Candidates

(Program Name from Step EXEC=)

SYSG (1 of 2)



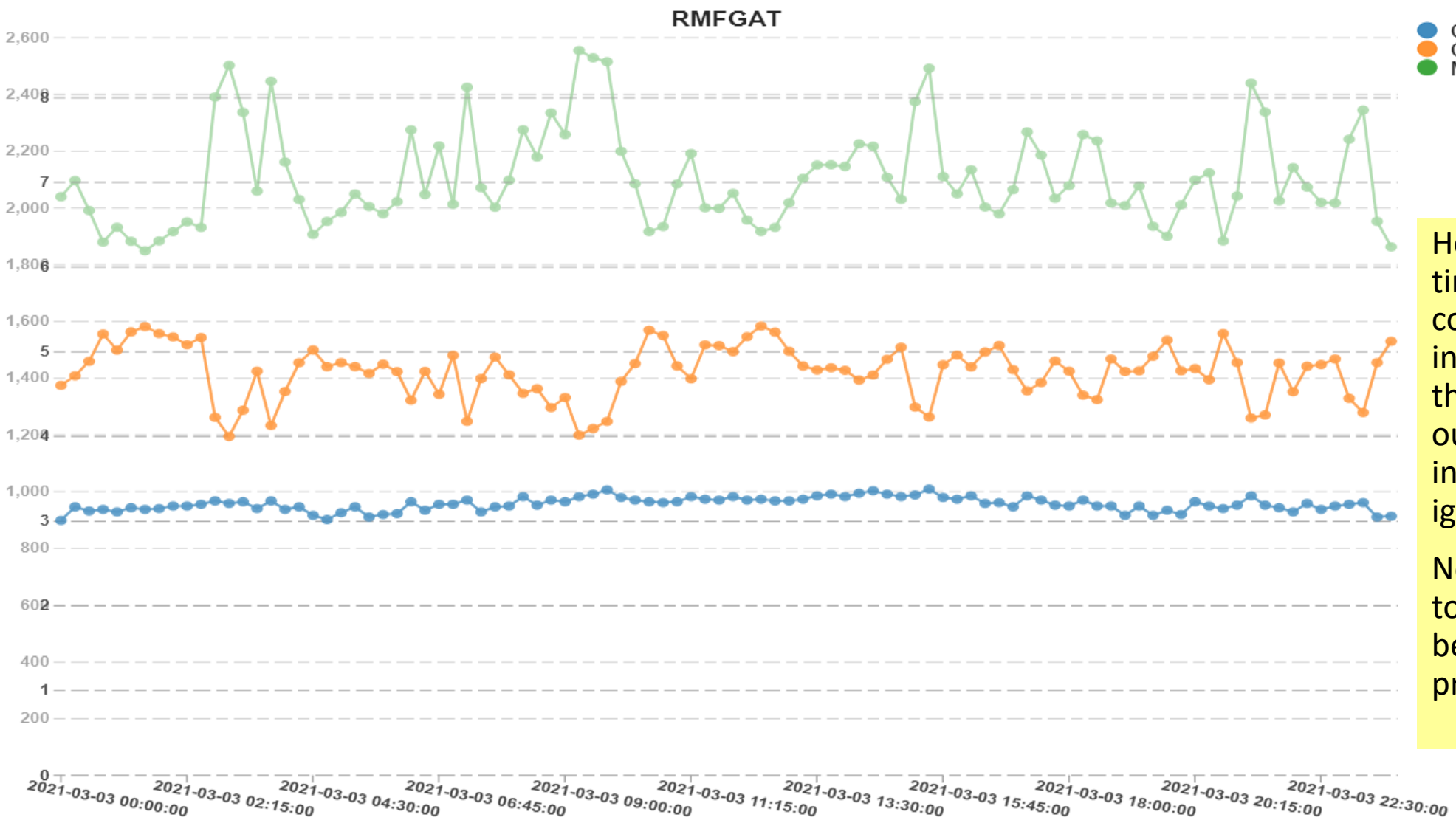
Interesting possibility here that *maybe* some SAS activity is driving some of the high SIIS %.

Can we trust SMF 30 CPI?

- Short answer: “no”
- Long answer: “no, but it *may* still be useful for finding SIIS culprits”

- Address space CPI depends on the cycle counts in the SMF 30 records
- Already mentioned the variability problem
- One thought has been “ignore the obviously bad measurements”
  - But if some are obviously bad, are there others that are less obviously bad?
  - I think the answer has to be yes (in most systems)
- Even given the variability, address spaces/programs that *consistently* show higher than expected CPI during times of high SIIS% might be worth investigating

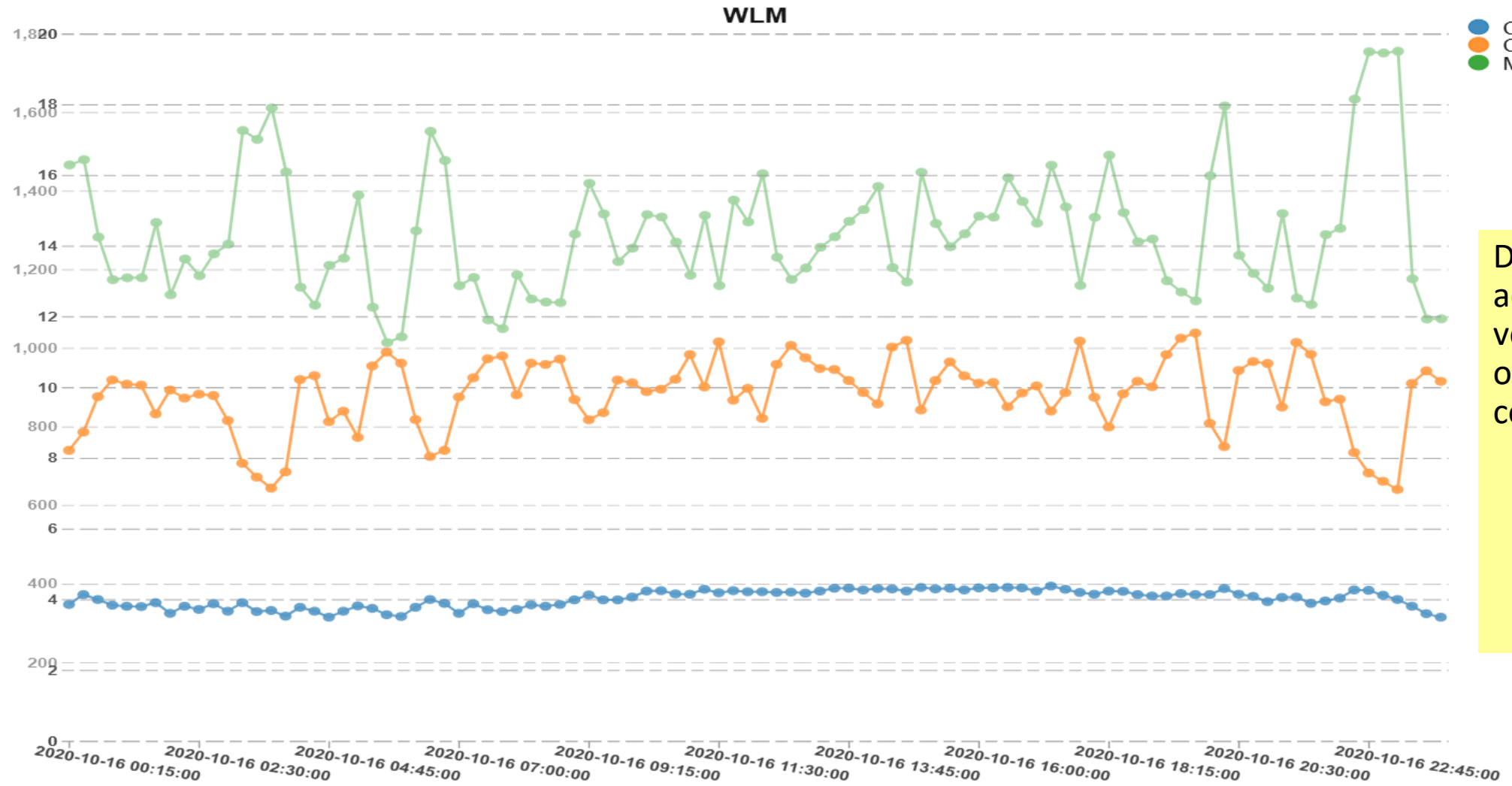
Address Space Instruction Details



Here RMFGAT's CPU time is definitely more consistent than its instruction count and there's no real obvious outliers in terms of the instruction counts to ignore.

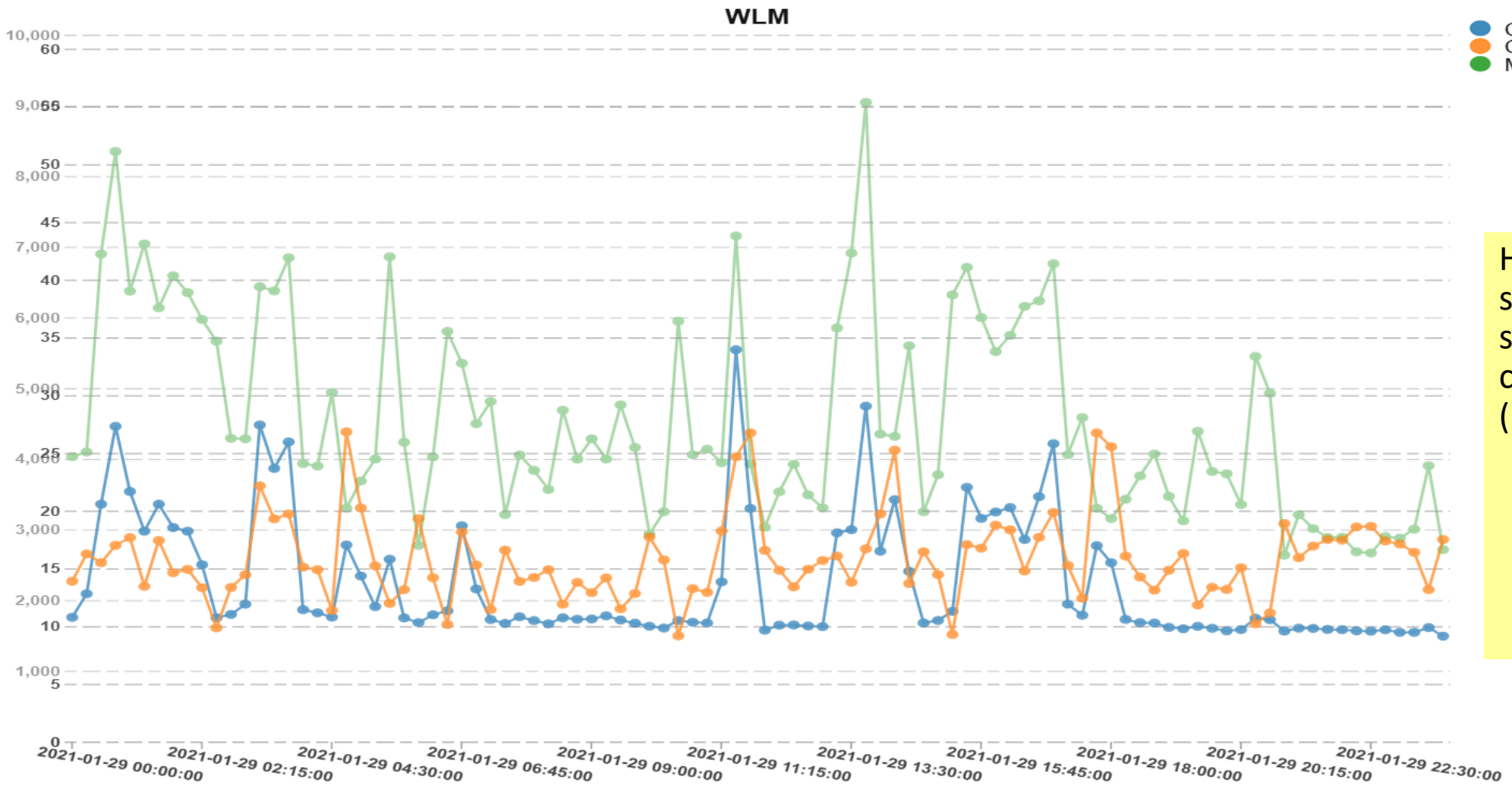
Note CPI varies inversely to instruction count because CPU time is pretty consistent.

Address Space Instruction Details



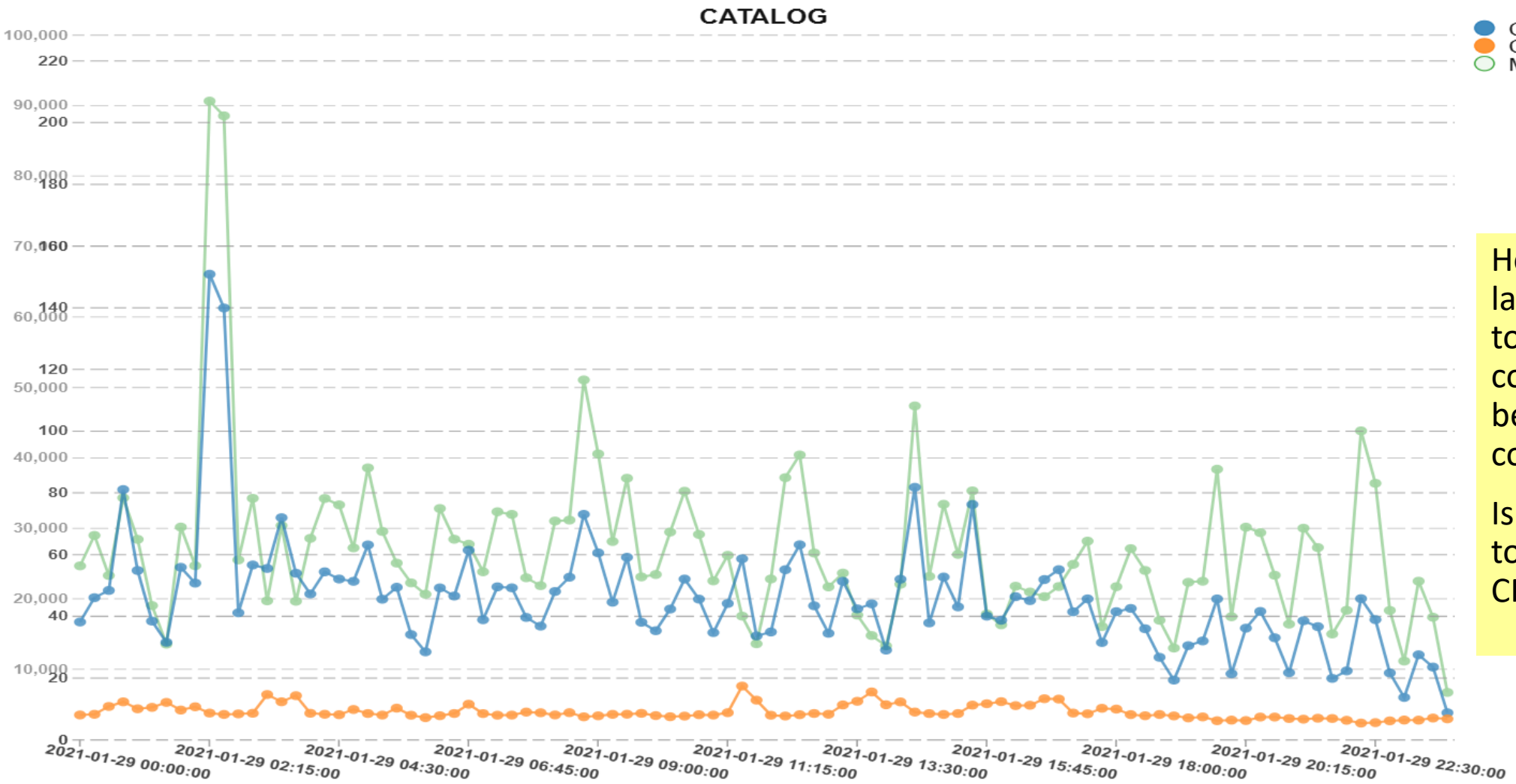
Different system, WLM address space consumes very consistent amount of CPU but instruction count varies significantly.

Address Space Instruction Details



Here's WLM on a larger system. There does seem to be better correlation here in most (but not all!) intervals.

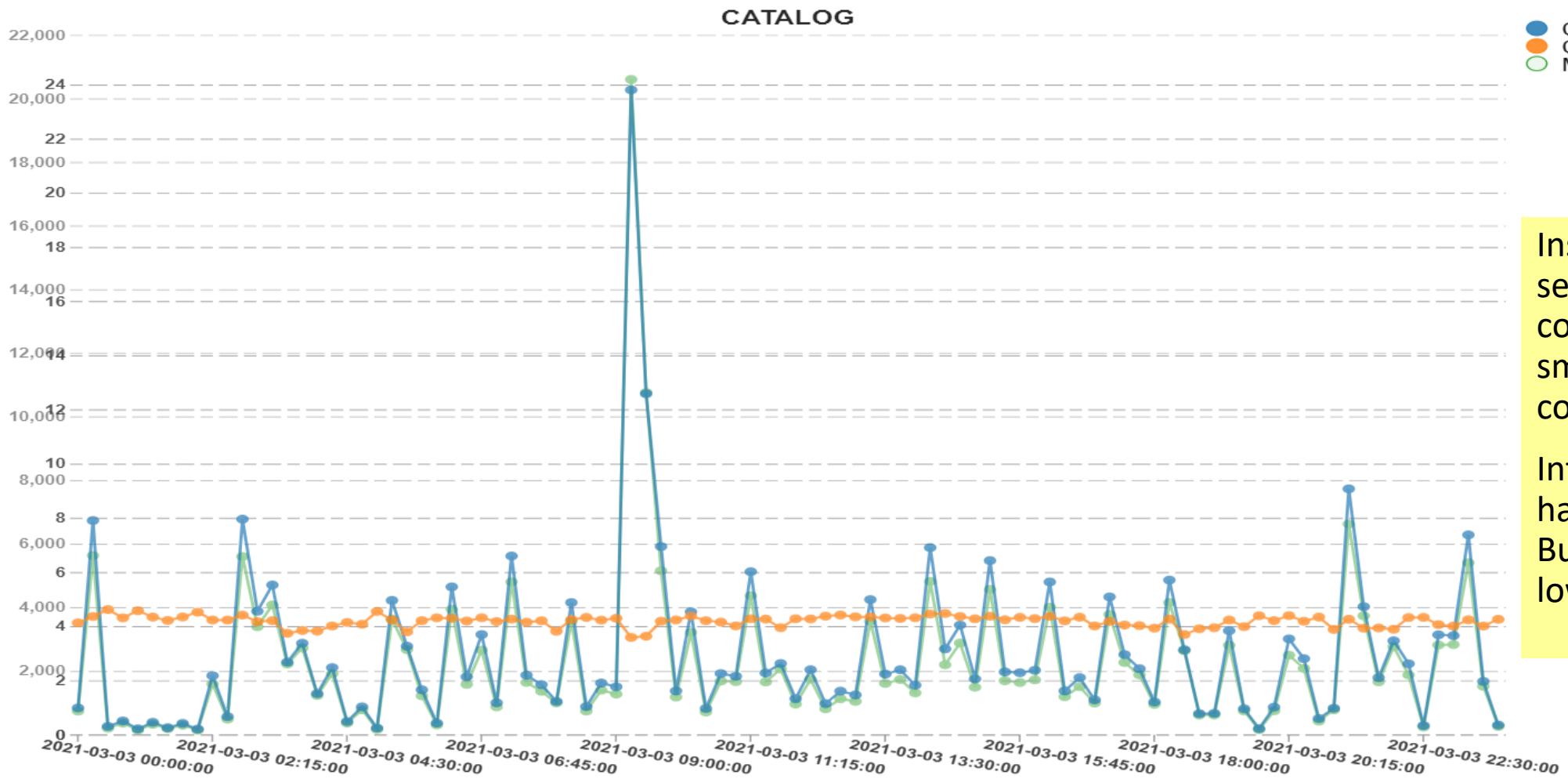
Address Space Instruction Details



Here's CATALOG on that larger system: it seems to have a more consistent relationship between instruction counts and CPU time.

Is this good luck or due to consuming more CPU?

Address Space Instruction Details



Instructions and CPU seconds extremely well correlated on this smaller system: best correlation I've found!

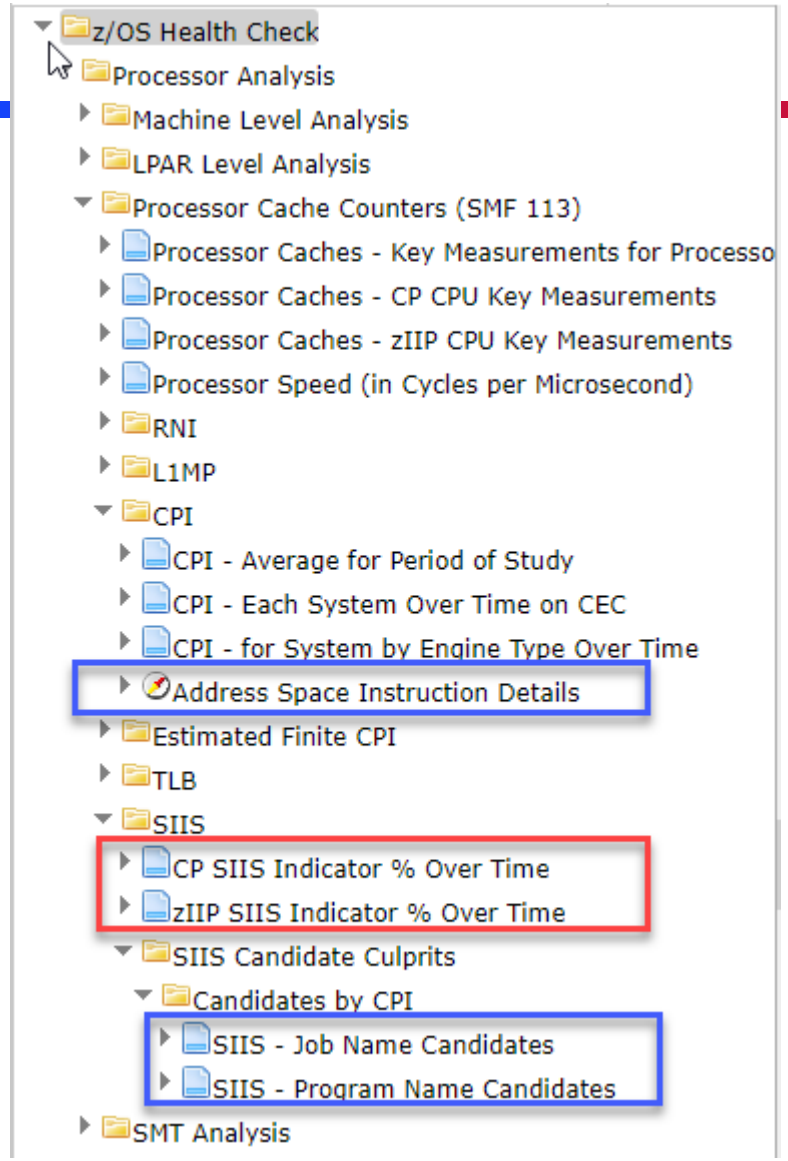
Interestingly(?) this LPAR had a single logical CP. But also had relatively low interrupt rate.

Conclusions

- Only worry about SIIS % Indicator in intervals with significant CPU usage
  - Also consider the type and diversity of work running in the interval
- Look first for what's running during those intervals
  - Customers without Assembler application code generally have few SIIS problems
    - Most ISV code has been fixed
- SMF 30 instruction counts *might* help you find the culprits that are driving up the SIIS % Indicator
  - SMF 30 instruction counts are variable to degrees that are not always obvious
  - LPARs with low I/O rates *may* be less susceptible to this issue
  - Don't assume high CPIs based on the SMF 30 data is indicative of a problem
  - If you aren't having a SIIS % problem, there still seems to be little need to turn on the SMF 30 instruction counts

For Pivotor Customers…

- Find those new reports under the Processor Cache Counter section
- Note the reports outlined in blue are dependent on the SMF 30 instruction counts and won't appear if you don't have those enabled
- If you have any questions, don't hesitate to reach out!



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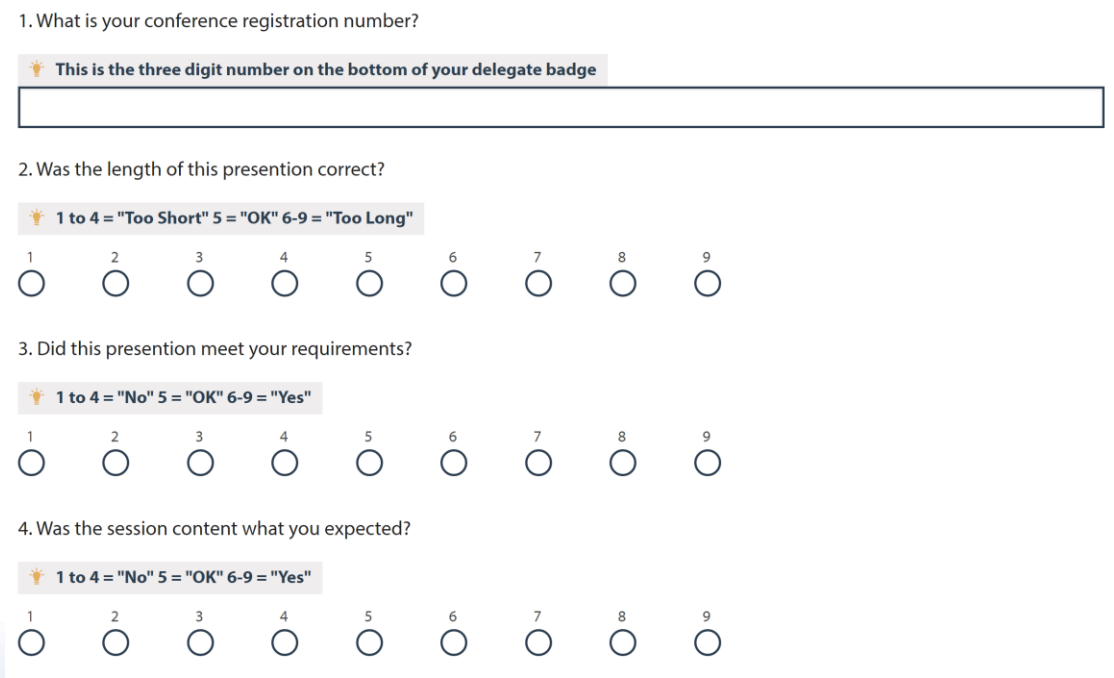

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